AMENDMENTS TO THE CLAIMS

Claim 1 (original): In a pseudo-random sequence generator having a linear feedback shift register (LFSR) that has a plurality of stages connected so as to generate a first pseudo-random sequence at an output of the last stage of the LFSR and to generate a sequence of vectors each constituting the output of at least some of the stages of the LFSR, a method comprising the steps of:

selectively combining vector values of each vector of the sequence of vectors in a first way to produce a second pseudo-random sequence;

selectively combining vector values of each vector of the sequence of vectors in a second way to produce a third pseudo-random sequence; and

selectively outputting bits of the second pseudo-random sequence and at least one bit of the third pseudo-random sequence to form a fourth pseudo-random sequence, wherein the fourth pseudo-random sequence differs from the first pseudo-random sequence.

Claim 2 (original): The method of claim 1, wherein the step of selectively outputting comprises:

outputting the bits of the second pseudo-random sequence until one of the vectors of the sequence matches a pre-determined value; and

outputting the at least one bit of the third pseudo-random sequence.

Claim 3 (original): The method of claim 1, wherein the step of selectively combining vector values of each vector of the sequence of vectors to produce the second pseudo-random sequence comprises the step of exclusive-ORing a first set of vector values of each vector of the sequence of vectors.

Claim 4 (original): The method of claim 3, wherein the step of selectively combining vector values of each vector of the sequence of vectors to produce the third pseudo-random sequence comprises the step of exclusive-ORing a second set of vector values of each vector of the sequence of vectors wherein the second set of vector values is different from the first set of vector values.

Claim 5 (original): The method of claim 1, wherein the LFSR comprises N stages, and wherein the first pseudo-random sequence, the second pseudo-random sequence, the third pseudo-random sequence and the fourth pseudo-random sequence each comprise at most 2^N bits.

Claim 6 (currently amended): A pseudo-random sequence generator, comprising:

a linear feedback shift register (LFSR) having a plurality of stages, the LFSR generating a first pseudo-random sequence and generating a sequence of vectors each constituting the output of at least some of the stages of the LFSR;

a first mask circuit coupled to receive the sequence of vectors, the first mask circuit generating a second pseudo-random sequence by selectively combining vector values of each vector of the sequence of vectors;

a second mask circuit coupled to receive the ~~LFSR state vector~~sequence of vectors, the second mask circuit generating a third pseudo-random sequence by selectively combining vector values of each vector of the sequence of vectors; and

logic circuits for generating a fourth pseudo-random sequence from the second pseudo-random sequence and the third pseudo-random sequence, wherein the fourth pseudo-random sequence comprises bits of the second pseudo-random sequence and at least one bit of the third pseudo-random sequence.

Claim 7 (currently amended): The pseudo-random sequence generator of claim 6, wherein the logic circuits comprise:

a multiplexer coupled to the first mask circuit and the second mask circuit to receive the second pseudo-random sequence and the third pseudo-random sequence; and

a control circuit coupled to the LFSR to receive the sequence of vectors, and wherein the control circuit is configured for controlling the multiplexer to output the bits of the second pseudo-random sequence until one of the vectors of the sequence matches a pre-determined value, and for controlling the multiplexer to output at least one bit of the ~~second~~ third pseudorandom sequence when one of the vectors matches the pre-determined value.

Claim 8 (original): The pseudo-random sequence generator of claim 6, wherein the first mask circuit is configured for exclusive-ORing a first set of vector values of each vector of the sequence of vectors to generate the second pseudo-random sequence.

Claim 9 (original): The pseudo-random sequence generator of claim 8, wherein the second mask circuit is configured for exclusive-ORing a second set of vector values of each vector of the sequence of vectors to generate the third pseudo-random sequence, where the second set of vector values is different from the first set of vector values.

Claim 10 (original): The pseudo-random sequence generator of claim 6, wherein the LFSR comprises N stages, and wherein the first pseudo-random sequence, the second pseudo-random sequence, the third pseudo-random sequence and the fourth pseudo-random sequence each comprise at most 2^N bits.

Claims 11-14 (canceled)

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Claim 15 (currently amended): A method of operating a linear feedback shift register (LFSR) having a plurality of stages connected so as to generate a pseudo-random output sequence at an output of a last stage of the LFSR, said method comprising:

generating a sequence of vectors, each vector constituting the output of at least some of the stages of the LFSR;

selectively combining vector values of each vector of the sequence of vectors ~~of the vectors~~ in a first way to produce a first sequence;

selectively combining the vector values of each vector of the sequence of vectors in a second way to produce a second sequence; and

selectively combining the first sequence and the second sequence to produce a third sequence that differs from the pseudo-random output sequence.

Claim 16 (original): The method of claim 15, wherein the step of selectively combining vector values in a first way comprises exclusive-ORing a first set of vector values each vector of the sequence of vectors.

Claim 17 (original): The method of claim 16, wherein the step of selectively combining vector values in a second way comprises exclusive-ORing a second set of vector values of each vector of the sequence of vectors.

Claim 18 (original): A pseudo-random sequence generator, comprising:

a linear feedback shift register (LFSR) comprising a plurality of stages connected so as to generate a pseudo-random output sequence at an output of a last stage of the LFSR and to generate a sequence of vectors, each vector constituting the output of at least some of the stages of the LFSR;

first logic for selectively combining vector values of each vector of the sequence of vectors in a first way to produce a first sequence;

second logic for selectively combining the vector values of each vector of the sequence of vectors in a second way to produce a second sequence; and

third logic for selectively combining the first sequence and the second sequence to produce a third sequence that differs from the pseudorandom output sequence.

Claim 19 (original): The pseudo-random sequence generator of claim 18, wherein the first logic comprises a first mask circuit configured for exclusive-ORing a first set of the vector values of each vector of the sequence of vectors.

Claim 20 (original): The pseudo-random sequence generator of claim 19, wherein the second logic comprises a second mask circuit configured for exclusive-ORing a second set of the vector values of each vector of the sequence of vectors .

Claim 21 (canceled)

Claim 22 (original): The pseudo-random sequence generator of claim 18, wherein the third logic comprises:

a multiplexer coupled to the first logic and the second logic to receive the first sequence and the second sequence; and

a control circuit coupled to monitor the sequence of vectors, and wherein the control circuit is configured for controlling the multiplexer to output the first sequence until one of the vectors of the sequence matches a pre-determined value, and for controlling the multiplexer to output the second sequence when one of the vectors of the sequence matches the pre-determined value.